REMARKS

In a final Office Action dated March 3, 2004 (paper no. 6), the Examiner rejected claims 1-6 under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium. The Examiner rejected claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz et al. (U.S. patent no. 6,334,197, hereinafter referred to as "Eroz"). The rejections and objections are traversed and reconsideration is hereby respectfully requested.

The Examiner rejected claims 1-6 under 35 U.S.C. §101 as being directed to an algorithm and not embedded in a computer readable medium, noting that the steps therein are directed to mathematical algorithms rather than limited to practical applications. In accordance with the suggestion of the Examiner, the applicants have amended claim 1 to direct the claim to an interleaving method for interleaving data elements in a communication system employing turbo codes. Accordingly, the applicants respectfully request that the Examiner withdraw the rejection of claims 1-6 under 35 U.S.C. §101. The applicants contend that the amendment of claim 1 does not necessitate a new search as the method claimed by claim 1 is already included in the interleavers of claims 7 and 14.

The Examiner rejected claims 7-19 under 35 U.S.C. §103(a) as being unpatentable over Eroz. Specifically, with respect to claims 7, 13, and 14, the Examiner contended that Eroz teaches a two dimensional block interleaver (element 16 in FIG. 2) comprising a number of rows and a number of columns, wherein data is read into the interleaver row-by-row, then row and column permutations are performed to randomize data positions, and then the data is read out column-by-column (col. 9, lines 2-10). Specifically, the Examiner noted that Eroz teaches for an input position '$1 = C * i + j$,' a corresponding output position is '$I(1) = R*\Pi_i(j) + \rho(i)$,' where '$\Pi_i$' is a column permutation application to data in row I and 'ρ' is bit reversed indexing (col. 9, lines 11-17). The Examiner acknowledged that Eroz does not disclose a controller configured to bit reverse row and column indices. However, the Examiner contended that it would have been well known

to one of ordinary skill in the art that controllers are required in order to perform read and write operations for forward or backward (bit reversing) operations.

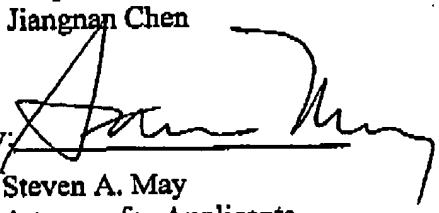
The applicants respectfully disagree with the Examiner's interpretation of Eroz. In the interleaver of Eroz, for an input position '1 = C * i + j,' a corresponding output position is '$I(1) = R*\Pi_i(j) + \rho(i)$,' where '$\rho(i)$' is the bit reversal pattern for the i^{th} row and '$\Pi_i(j)$' is a column permutation applied to the data in the i^{th} row. While '$\Pi_i(j)$' is a column permutation pattern, it is not done with bit reversals for the columns as in claims 1, 7, 13, and 14. Instead, Eroz implements the column permutation pattern by use of Galois field arithmetic, which is extremely difficult to implement and which results in a totally different pattern than the bit reversal indexing of claims 1, 7, 13, and 14. Furthermore, while Eroz provides a bit reversal index '$\rho(i)$' for each row, each of claims 1, 7, 13, and 14 goes beyond Eroz by providing a row shifting operation for each row with a specific pattern after bit reversal indexing.

Therefore, it is no surprise that the relationship between the starting interleaver matrix (the matrix on page 6, line 12 of the pending application and matrix 8 in Eroz) and the final interleaver matrix (the matrix on page 7, line 9 of the pending application and matrix 17 in Eroz) is completely different between the pending application and Eroz and results in different final distances of adjacent input values, as the method of interleaving/interleaver of claims 1, 7, 13, and 14 use bit-reversal combined with a shifting operation that results in a completely distribution of the transmitted bits. Eroz does not teach the limitations of claims 1, 7, 13, and 14 of bit reversing row indexes for a first predetermined number of rows and permuting the corresponding data elements, bit reversing column indexes for a second predetermined number of columns and permuting the corresponding data elements, and shifting bit storage locations of one or more of the first predetermined number of rows a respective predetermined number of columns. Accordingly, the applicants respectfully request that claims 1, 7, 13, and 14 may now be passed to allowance.

Since claims 2-6 depend upon allowable claim 1, claims 8-12 depend upon allowable claim 7, and claims 15-19 depend upon allowable claim 14, the applicants respectfully request that claims 2-6, 8-12, and 15-19 may now be passed to allowance.

As the applicants have overcome all substantive rejections and objections given by the Examiner and have complied with all requests properly presented by the Examiner, the applicants contend that this Amendment, with the above discussion, overcomes the Examiner's objections to and rejections of the pending claims. Therefore, the applicants respectfully solicit allowance of the application. If the Examiner is of the opinion that any issues regarding the status of the claims remain after this response, the Examiner is invited to contact the undersigned representative to expedite resolution of the matter.

Respectfully submitted,
Jiangnan Chen

By: 

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